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Experimental characterization of electrical current leakage in poly(dimethylsiloxane) microfluidic devices

Jiashu Sun · Saumitra K. Vajandar · Dongyan Xu · Yuejun Kang · Guoqing Hu · Dongqing Li · Deyu Li

Abstract Poly(dimethylsiloxane) (PDMS) is usually considered as a dielectric material and the PDMS microchannel wall can be treated as an electrically insulated boundary in an applied electric field. However, in certain layouts of microfluidic networks, electrical leakage through the PDMS microfluidic channel walls may not be negligible, which must be carefully considered in the microfluidic circuit design. In this paper, we report on the experimental characterization of the electrical leakage current through PDMS microfluidic channel walls of different configurations. Our numerical and experimental studies indicate that for tens of microns thick PDMS channel walls, electrical leakage through the PDMS wall could significantly alter the electrical field in the main channel. We further show that we can use the electrical leakage through the PDMS microfluidic channel wall to control the electrolyte flow inside the microfluidic channel and manipulate the particle motion inside the microfluidic channel. More specifically, we can trap individual particles at different locations inside the microfluidic channel by balancing the electroosmotic flow and the electrophoretic migration of the particle.

Keywords Microfluidics · Current leakage · PDMS · Particle trapping/concentration · AC pumping

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1 Introduction

Microfluidic systems provide a promising and powerful platform for biological and chemical analysis, with the merits of less sample consumption, higher throughput, and lower cost (Reyes et al. 2002; Beebe et al. 2002). One important issue in microfluidic systems is how to control and manipulate the motion of analyte samples. Electrokinetic methods, because of their fast response, simple implementation, and easy automation, have been widely adopted in the development of lab-on-a-chip devices (Bousse et al. 2000; Li 2004).

The most common electrokinetic methods include electroosmotic, electrophoretic, and dielectrophoretic sample handling. Electroosmotic flow can be induced when a microfluidic channel is filled with an electrolyte and an external electric field is applied along the channel axial direction. At the interface of the channel wall and the electrolyte, a layer of fixed surface charge and a diffuse layer of electrolyte rich in mobile counter-ions will form an electric double layer (EDL). The external electric field will drive the counter-ions in the EDL to move, dragging the bulk liquid to flow. Electroosmotic flow has been widely used to manipulate analyte samples (Li 2004). Electrophoretic and dielectrophoretic forces have also been widely used to manipulate various types of samples such as particle/cell trapping and separation (Green et al. 1997; Fiedler et al. 1998; Gascoyne 2002), sample pre-concentration (Lichtenberg et al. 2001; Stroink et al. 2001; Asbury et al. 2002), and DNA/protein separation (Heller 2001; Xu et al. 2002; Gao et al. 2001; Doherty et al. 2003).

Most microfluidic devices are fabricated using silicon, glass, and polymeric materials. Poly(dimethylsiloxane) (PDMS), which is elastic, optically transparent, nontoxic, and biologically compatible, has been extensively used in

lab-on-a-chip devices because they can be easily fabricated by the soft-lithography technique at low cost (Duffy et al. 1998; McDonald et al. 2002).

Although PDMS has a low breakdown voltage (about 21 V/μm) (McDonald et al. 2002), it is usually considered a dielectric material and the PDMS microchannel wall is treated as an electrically insulated boundary in an applied electric field (Choi and Park 2005; Mineta et al. 2008). With the rapid development of the lab-on-a-chip technology, more complex microfluidic circuits are integrated into the limited space on a single microchip (Thorsen et al. 2002). The large-scale integration leads to adjacent microchannels with very narrow separation in between. When the separation distance between microchannels goes down to tens of microns or even smaller, it may no longer be appropriate to consider the PDMS material as perfectly insulating because of the potential electrical leakage through the thin PDMS wall. For example, considering a PDMS-glass microchip that has two parallel microchannels with a separation distance of tens of microns, if an electric potential difference exists between these two channels, a leaking current could be generated through the thin PDMS wall. Although such leaking current is normally very small, it could be comparable and contribute significantly to the already very low current in the fluidic channel, and therefore, could significantly alter the electric field in the microfluidic circuits.

Current leakage through PDMS channel walls has been reported in the literature. Horiuchi and Dutta (2006) recently developed a leaking current model for field-effect control of flow in PDMS microchannels and claimed that the zeta potential could be changed to realize flow control using relatively low gate voltage. However, data of leaking current through PDMS are still limited and further investigation is needed to clarify the leakage through PDMS structures in microfluidic circuits. Characterization of current leakage through PDMS is of increasing interest and importance as microfluidic circuits are getting more complex with multi-channel designs to achieve multi-functions.

In this paper, we report on our characterization of the current leakage through PDMS walls. Based on the measured leaking current data, we simulated the effects of the current leakage on the electric field within the microchannel. Furthermore, we used current monitoring method to determine whether field-effect control could be easily realized to adjust the zeta potential and thus the electroosmotic flow in microfluidic channels made of PDMS. With the acquired knowledge of the current leakage, we then explored the possibility of trapping particles by the electrostatic effect resulted from the leaking current in a microchannel with a gate electrode. In addition, we observed net flow in the main channel induced by AC electroosmosis with asymmetric side channels in the vicinity of the main channel as electrodes.

2 Device fabrication

The microfluidic devices are fabricated using standard soft-lithography techniques (Sia and Whitesides 2003) on PDMS-glass chips. Molds were created on 3-inch silicon wafers that were first thoroughly cleaned with Piranha (75% H_2SO_4:25% H_2O_2) and dehydrated at 200°C on a hot plate. SU-8 2015, or SU-8 2025 photoresists (MicroChem Corp, MA) were then spin-coated on the wafers at 500 rpm for 10 s, followed by 3,000 rpm (SU-8 2015), 3,000 rpm (SU-8 2025), or 2,000 rpm (SU-8 2025) for 30 s, respectively, to obtain different thicknesses of 15, 30, and 45 μm. The coated wafers were soft-baked at 95°C for 5 min. The photoresist was then exposed to ultraviolet light through photomasks for appropriate times, followed by post-exposure bake (PEB) at 95°C for 5 min. Finally, SU-8 developer (MicroChem Corp, MA) was used to dissolve the photoresist in unexposed regions.

After the SU-8 mold was hard baked, the PDMS prepolymer and the curing agent (Sylgard 184, Dow Corning Inc, MI) were mixed at a ratio of 10:1 and poured over the SU-8 master on the silicon wafer that was fixed in a petri dish to obtain a 5 mm thick slab. The mixture of PDMS elastomer was then degassed for 2 h at 0.001 torr and heated in an oven at 80°C for 3 h. The solidified PDMS slab was peeled off from the silicon wafer and punched at specified locations to form wells. Finally, the PDMS slab and a glass slide were exposed to oxygen plasma for 30 s, and brought into contact quickly to seal the microchannels to form desired devices.

3 Results and discussion

We selected 15-μm thick walls to test the electrical leakage because they were the thinnest PDMS walls we could make by low-cost soft-lithography without using much more expensive solid-state fabrication facilities. We also tested the leakage current through 50 μm thick PDMS walls because the leakage current through 50 μm thick walls have been discussed in the literature.

3.1 Characterization of current leakage through PDMS structures

Figure 1 shows the basic structure of the chip design for measuring the leakage current. In this experiment, there are four different configurations of a main (center) channel sandwiched between two side channels, which are symmetric and separated from the main channel by a 15 μm thick PDMS channel wall. Three of the four configurations vary only in dimension, while the fourth configuration has a different structure.
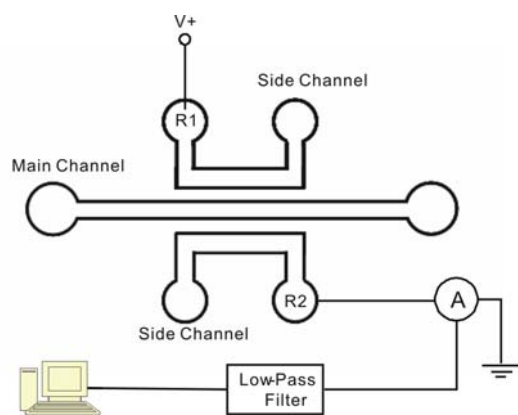
Fig. 1 Schematic diagram of leakage current measurement in the PDMS-based microdevice

The first three chips all have 100 μm wide, U-shaped symmetrical side channels and the main channels are 100 and 18,000 μm wide and long, respectively. The lengths of the side channels of the three chips are different, which are 100, 500, and 2,000 μm, respectively. In addition, the channel depth in the third chip is 45 μm, greater than that for the first two chips (30 μm).

The fourth configuration (Fig. 2) has two-three-pronged symmetrical side channels, which is also used for the particle trapping experiment later. In the center region, the width of the main channel shrinks from 100 to 15 μm, forming a particle trapping section which has a dimension of 15/2,000 (width/length, μm). The overall main channel is 1.8 cm long and the bulk region is 100 μm in width. The parallel side channels and the particle trapping section in the main channel have the same length and are separated by 15 μm thick PDMS walls. All the channels are 15 μm in depth.

The microfluidic devices were filled with 10 mM sodium borate buffer (the buffer conductivity was measured by a conductivity meter (Eutech Instruments, IL) as 0.16 S/m). A positive voltage was applied to the left-side well (R1) of the top side channel and the right-side well
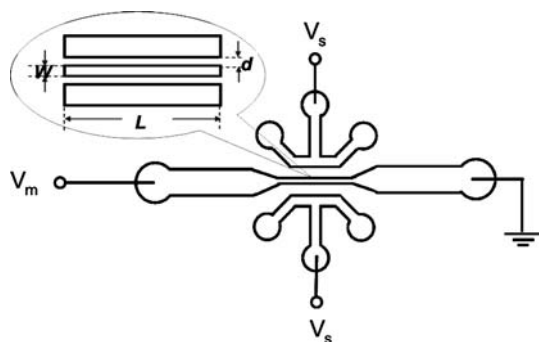
(R2) of the bottom side channel is grounded. The leakage current was measured with a current preamplifier (Model 1211, DL Instruments, NY), which was fed into the data acquisition system after being processed with a low-pass filter (Model SR560, Stanford Research Systems, CA).

Figure 3 shows the measured leakage current through the two wells (R1 and R2) under applied voltages ranging from 10 to 50 V for the four different side channels. Also shown in Fig. 3 is the linear fit to the experimental data. It is clearly shown in Fig. 3 that a linear relationship exists between the applied voltage and electrical leakage current. In such configuration, the total electrical resistance consists of four parts: the upper channel's resistance, the PDMS walls' resistance, the main channel's resistance, and the lower channel's resistance. In the present set-up, because of the complex configuration, and therefore, non-uniform electrical potential distribution in the channel, it is difficult to accurately estimate the total resistance from the electrolyte filled channel. In our calculation of the leakage conductivity of the PDMS channel wall, we take all the measured resistance as the resistance from the PDMS channel wall, which is a conservative estimation of the lowest leakage conductivity. This is because considering the channel resistance will only reduce the PDMS channel wall resistance and lead to a higher leakage conductivity.

Table 1 summarizes the electrical resistance and conductivity of the PDMS walls. Compared to the electrical conductivity of bulk PDMS (2.5×10^{-14} S/m) (Mark 1999), the measured leakage electrical conductivity of the thin (15 μm) PDMS structure in our devices is significantly larger (about 1.2×10^9 to 1.9×10^{10} times of the bulk value). Note that the leakage conductivity can vary by up to one order of magnitude for different cases, which may be due to the variation in the fabrication process.

Moreover, a 50 μm thick channel wall was used to investigate the effect of PDMS wall thickness on electrical leakage current. The device configuration was the same as the one discussed in Sect. 3.2, as shown in Fig. 4. The measured leakage conductivity of 50 μm thick channel wall was 1.33×10^{-5} S/m, which was lower than that of the 15 μm thick channel wall (3.0×10^{-5} S/m). It can be concluded that current leakage increases when the PDMS wall becomes thinner.

Furthermore, we have performed tests using PDMS/PDMS (PDMS channel bonded with PDMS substrate) chips and observed that the current leakage still existed. However, the leakage conductivity of PDMS/PDMS chips was 3–20 times lower than that of PDMS/glass chips.

Several possible reasons could explain such high conductivity of PDMS thin slabs and its variation from chip to chip. The bonding interface between the PDMS and the glass substrate may have nanometer scale pores because of the surface roughness of both PDMS and the substrate.

Fig. 2 Schematic of microfluidic chips for testing the leakage current and for particle trapping

Fig. 3 Measured leaking current and the fitting curves of current versus voltage through PDMS channel walls for four different side channel geometries (length of horizontal section × width × depth):
a $100 \times 100 \times 30\ \mu m^3$,
b $500 \times 100 \times 30\ \mu m^3$,
c $2{,}000 \times 100 \times 15\ \mu m^3$, and
d $2{,}000 \times 100 \times 45\ \mu m^3$
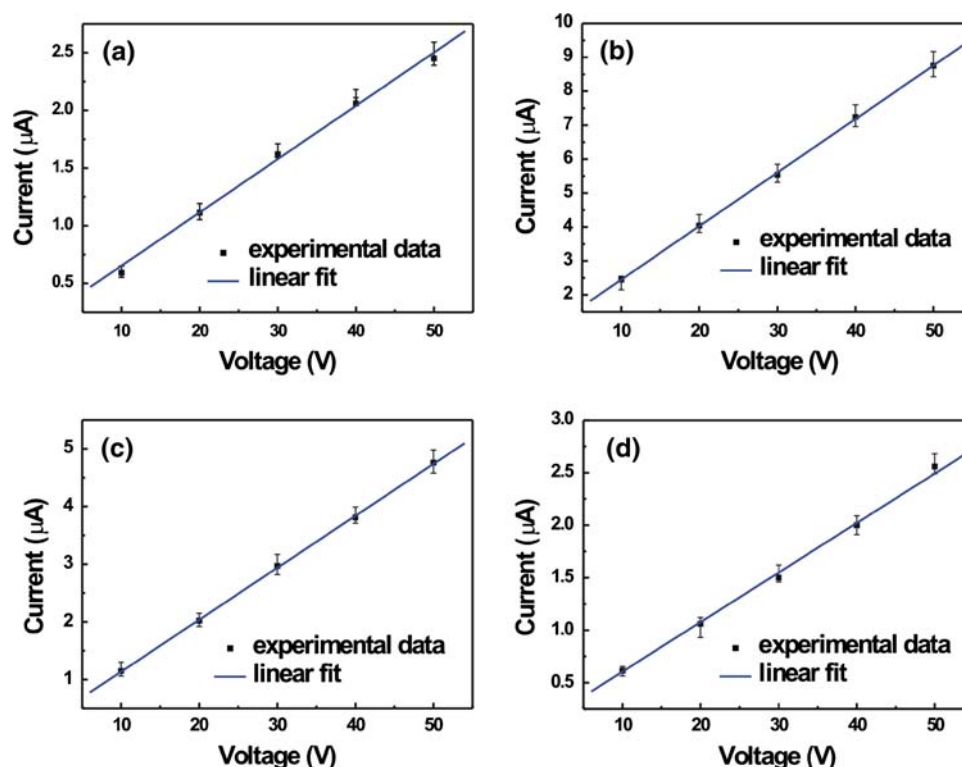
Table 1 Summary of measured electrical conductivity of small PDMS structures in the microfluidic devices

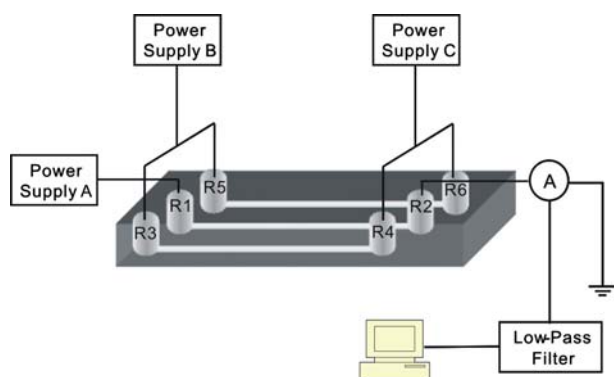| Geometry (width/length/ depth, μm)	Resistance (Ω)	Conductivity (s/m)
15/100/30	2.14×10^7	4.67×10^{-4}
15/500/30	6.33×10^6	3.16×10^{-4}
15/2,000/45	1.11×10^7	3.00×10^{-5}
15/2,000/15	2.06×10^7	4.85×10^{-5}

Fig. 4 Schematic diagram of the current monitoring to measure the EOF in the main microchannel under an applied gate voltage

These nanometer scale roughness may be enlarged during the oxygen plasma treatment. Such surface imperfection is negligible in the bulk portion of the bonded interface; however, for thin PDMS slab of tens of microns thick, the surface imperfections could render significant current leakage through the bonding interface. Because the surface imperfections were random, the leakage conductivity we measured varied significantly from chip to chip. In addition, PDMS is a material with numerous pin-holes that might also allow significant leakage current through thin channel PDMS structures.

In order to see if the electrical leakage was due to the poor bonding quality, fluorescent dyes (Bangs Laboratories Inc, IN) were put in the center channel of a PMDS/glass chip and a 40 V bias was applied across the channels for 1 h. No dye was observed in any of the side channels after the hour passed. Therefore, if the leakage current is from the bonding interface, it would be inherent of the PDMS/glass or PDMS/PDMS bonding in the soft-lithography technique, not due to poor bonding quality in our device fabrication.

3.2 Gating effects in PDMS microfluidic devices

Horiuchi and Dutta (2006) have recently reported gate control of the surface zeta potential in microfluidic device with 50 μm thick PDMS channel walls. They found that the zeta potential could be changed by tens of millivolts with applied gate voltages in the range of tens of volts. This could have important implications of using low-voltage gating effects to manipulate fluid flow and reagent delivery in microfluidic devices. In this section, we used current

monitoring technique to study the gating effects through PDMS channel walls.

As shown in the schematic diagram of the experimental set-up (Fig. 4), three DC power supply units (E3617A and E3612A, Agilent, CA) are used to provide designated voltages on the main channel and side channels. In this configuration, the main and side channels are of the same dimensions, which are 100/18,000/30 (width/length/depth, μm). They are separated by 50 μm thick PDMS channel wall. The current monitoring technique has been well-documented in the literature (Huang et al. 1988) and is only briefly introduced here. Initially a 10 mM sodium borate buffer was filled into the main channel and then the buffer in well R1 was sucked out and replaced with 9.5 mM borate buffer. The 9.5 mM borate buffer was driven into the main channel with electroosmotic pumping to replace the 10 mM borate buffer, which will lead to a decrease of the electrical current through the microchannel. The duration of the replacement event depends on the electroosmotic flow velocity of the buffer solution and thus can be used to estimate the zeta potential of the channel wall. We used the current monitoring technique to study the electroosmotic flow in the main channel both with and without gate voltages applied from the side channels.

For an isolated straight channel, the strength of the uniform electric field can be obtained by dividing the potential difference by the channel length. However, for a main channel with parallel side channels, due to the leaking current through the PDMS channel wall, the electric field in the main channel will be changed once a potential difference exists between the main channel and the side channels. Therefore, to create a uniform voltage difference between the side channel and the main channel along the axial direction of the main channel, an electrical potential of 80 V was applied to the upstream wells, R3 and R5, and an electrical potential of 30 V was applied to the downstream wells, R4 and R6, respectively, as shown in Fig. 4. The electrical bias across the main channel is fixed at 50 V, whether the gate voltage is applied to the side channels or not. All the power supplies are commonly grounded. This scheme of applying the gate voltage to the side channels helps to create a uniform voltage difference between the gate voltage in the side channels and the local voltage in the main channel, i.e., $\Delta V_g = V_g - V_{local}$ is designed to be 30 V everywhere. If there is any change of the zeta potential due to the gating effect, the change should be uniform along the channel.

Figure 5 shows the measured electrical current through the main channel as a function of time with and without the applied gate voltage. The current drops continuously until the entire electrolyte in the main channel is replaced with the 9.5 mM borate buffer. Even though the measured current is higher in the case with applied gate voltage, Fig. 5 indicates that the replacement time for both cases is
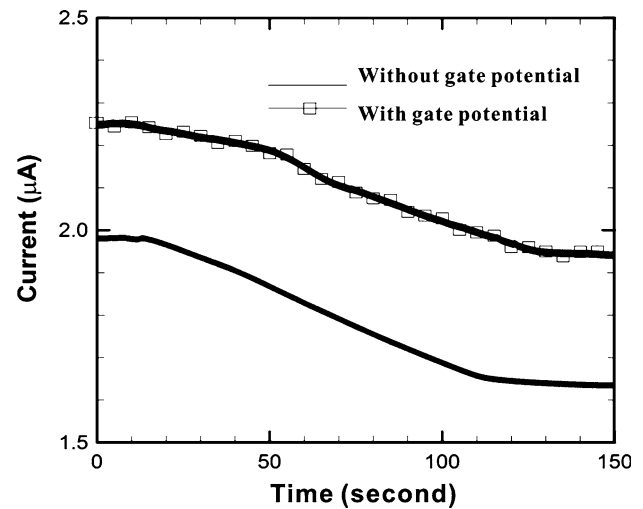

Fig. 5 Measured electroosmotic flow with the current monitoring method. The figure shows the current versus time curves for a 9.5 mM sodium borate buffer replacing a 10 mM sodium borate buffer in the main channel, without and with gate voltages applied in the side channels

almost the same (about 140 s) and the EOF velocity is calculated as 128 μm/s. The zeta potential at the channel wall can therefore be estimated to be about −68 mV, which agrees with the value in other published literature (Hsieh et al. 2006). From our results, we believe that the zeta potential was not modified by applying a moderate gate voltage (<100 V) across a PDMS wall that was tens of microns, different from the conclusions of Polson and Hayes (2000) and Horiuchi and Dutta (2006).

Horiuchi and Dutta (2006) developed a leakage capacitance model to estimate the modified zeta potential caused by the gate voltage in a PDMS microdevice. They modified the original equation of the zeta potential change under applied gate voltage, which is given by (Schasfoort et al. 1999).

$$\Delta\zeta = \frac{C_{wall}}{C_d}\Delta V_g \qquad (1)$$

as

$$\Delta\zeta = -\left(\frac{C_{total}}{C_{EDL2}}\right)\left(\frac{R_{leak}}{(R_{b3} + R_{leak}) + R_{b1}||R_{b2}}\right)\Delta V_g, \qquad (2)$$

where all the notations can be found in the original literature. The resistance term in Eq. (2) is a number always less than unity. Therefore, to have a significant zeta potential change with a moderate applied gate voltage, a large ratio of $\frac{C_{total}}{C_{EDL2}}$ is desired. The capacitance ratio $\frac{C_{total}}{C_{EDL2}}$ can be expanded as:

$$\frac{C_{total}}{C_{EDL2}} \approx \frac{C_{wall}}{C_{EDL2}} = \frac{\frac{A\varepsilon_0\varepsilon_w}{d}}{\frac{\varepsilon_b\varepsilon_0 A}{\lambda}\cos h\left(\frac{zF\zeta}{2RT}\right)} = \frac{\varepsilon_w\lambda}{\varepsilon_b d \cos h\left(\frac{zF\zeta}{2RT}\right)}, \qquad (3)$$

The calculated ratio from the above expression is on the order of 1.0×10^{-6}, which is substantially lower than

1.0×10^{-3} as given by Horiuchi and Dutta (2006). This may explain the different experimental observations. The difference in the capacitance ratio may originate from different experimental conditions. However, our results indicate that at least field-effect control in PDMS-based device with channel wall of tens of microns thick is not universal.

To further understand our results, we measured the leakage current in the device as shown in Fig. 4 and calculated the leakage conductivity of the 50 μm thick PDMS wall as about 1.33×10^{-5} S/m. Using these data, we simulated the electric field in the main channel, side channels, and the PDMS wall using a commercial finite element package Comsol 3.2 (Comsol, Inc. MA). The electric potential and electric field strength along the axial direction in the main channel is shown in Fig. 6, which indicates that the electric field can be significantly altered by the applied gate voltage due to the current leakage. In addition, we simulated the EOF and found that the overall flow rate in the main channel remains almost the same as in the case of no applied gate voltage. However, the alteration of the electric field does change the local flow field within the main channel.

Even though we did not observe gate modulation of the overall electroosmotic flow inside the microchannel made of PDMS, we found that the current leakage phenomena can be utilized for some interesting applications, as discussed in the following sections.

3.3 Particle trapping by altering the electrical field with leakage current

Manipulating particles inside microfluidic channels are of tremendous interest in microfluidic devices (Müller et al. 1996; Liu et al. 2006). The local electric field change because of the leakage current may be used for particle manipulation. The microfluidic device for this purpose is shown schematically in Fig. 2. The central section of the main channel is 2 mm long (L) and 15 μm wide (W) filled with 1 mM sodium borate buffer, which is separated by a 15 μm thick (d) PDMS channel wall from the side channel.

As discussed in the previous section, the current leakage from the side channel could alter the otherwise uniform electric field in the main channel. Based on the measured leakage current, we simulated the electric field in the main channel, side channels, and PDMS channel walls. The electric field is described by the Laplace equation with varied conductivities:

$$\nabla \cdot (\sigma_i \nabla V) = 0, \tag{4}$$

where σ_i represents the electrical conductivities of different regions in the simulation domain. According to the experimental measurement, the conductivity of 1 mM sodium borate buffer is around 0.01 S/m, and the leakage conductivity of 15 μm thick PDMS in the present device is around 3.0×10^{-5} S/m.

Furthermore, the electroosmotic flow in the main channel was also calculated by the Navier–Stokes equation:

$$\rho \vec{u} \cdot \nabla \vec{u} = -\nabla P + \eta \nabla^2 \vec{u}, \tag{5}$$

with the Helmholtz–Smoluchowski slip boundary condition at channel walls.

The above equation is numerically solved using the finite element package Comsol Multiphysics 3.2 (Comsol Inc., MA) for the case of 5 V electrical bias across the main channel ($V_m = 5$ V). It was found that when a negative potential was applied to the side channel, the electric field decreased from a positive value at the inlet to zero and then reversed its polarity to negative, due to the effect of leakage through PDMS, as plotted in Fig. 7. Even though the overall potential drop across the channel does not change, the local electric field is significantly different and much stronger. It is interesting that with the modified electrical field, we could trap individual particles inside the main channel with both negative and positive gate potential.

Fig. 6 Calculated potential and electric field distribution in the main channel with applied potential to the side channels: **a** electric potential, **b** electric field strength along x-direction (E_x)
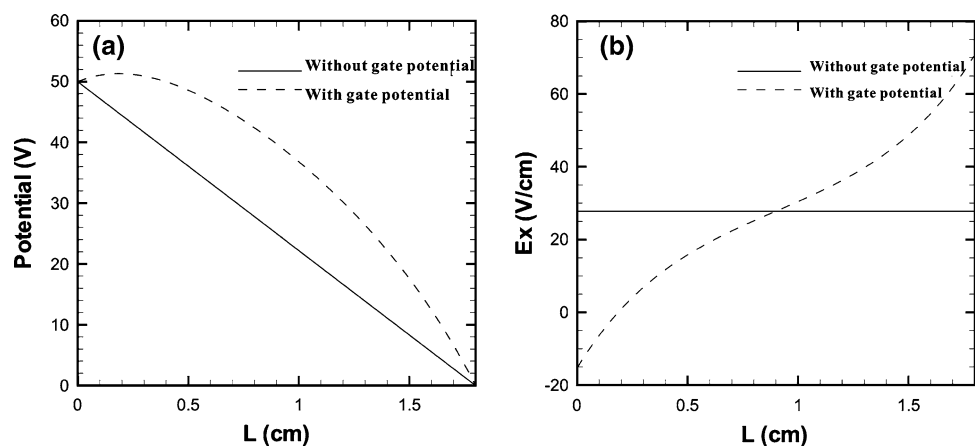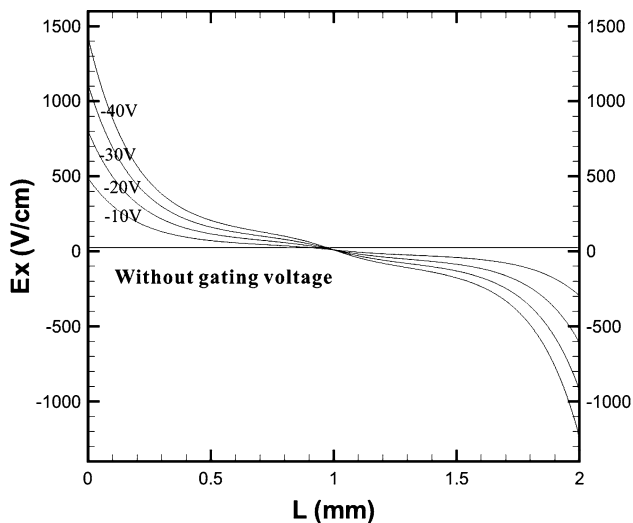
Fig. 7 Numerical predictions of the electric field strength under different negative gate voltages applied to the side channel
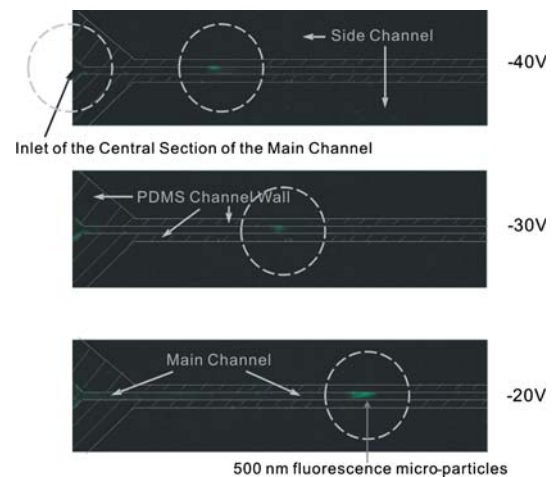

Fig. 8 Images of the fluorescence microparticle trapped using the leaking current with a negative applied voltage to the side channel
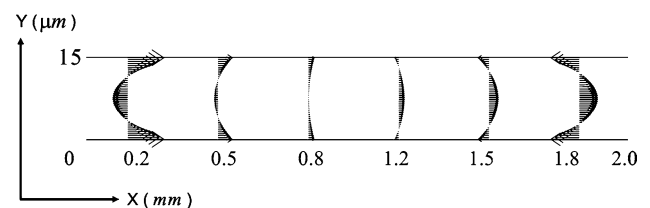

Fig. 9 Numerical results of the velocity profile at different locations in the main channel. The applied gate voltage is −40 V

We first conducted our experiments with 0.2% (V/V) liquid suspension of negatively-charged 500 nm fluorescent micro-particles (Bangs Laboratories Inc, IN) to demonstrate the particle trapping. Initially, a positive electric bias of 5 V was applied across the main channel, which induced electroosmotic flow through the main channel and filled the channel with negatively charged 500 nm fluorescent particles. When a negative potential (e.g., −20 V) was applied to the side channels, it was observed that only a small portion of particles remain at certain location and the particles at the upstream locations would flow back to the inlet, while the particles at the downstream locations would flow to the outlet. Once the applied gate potential was changed (e.g., to −30, −40, and −50 V), a new balance would be formed and the particles would be trapped at a different location. The motion of micro-particles was recorded using an inverted optical microscope (Eclipse TE2000-U, Nikon, USA). Figure 8 shows the fluorescent images of the particle trapped under different applied gate potentials. We also found that the particles could not be trapped within the microchannel under a gate voltage of −10 V because the electroosmotic flow was always stronger than the weak electrophoretic migration of the particle.

Since the gate voltage changes the local electric field inside the main channel, the flow field inside the channel is also modified by the altered electric field. Even though the overall flow rate does not change, the flow is much more complex and deviates from the plug flow profile for simple electroosmotic flow. Figure 9 shows the modeled flow field in the main channel and it can be clearly seen that a two-dimensional flow field has been developed in the main channel. We believe that the observed particle trapping is because the electroosmotic flow is balanced by the electrophoretic migration of the particle. In the experiment, we observed that when a negative gate potential was applied, the particles were trapped in the upstream of the channel, where the electrical field is positive and the electrostatic force on the particle is in the opposite direction of the electroosmotic flow. However, more experiments using particles of different sizes need to be performed to fully understand the detailed trapping mechanism in the complex two dimensional flow field.

The trapping mechanism worked equally well for positive gate voltage (higher than the total bias of the main channel) since the electrical field inside the main channel was also enhanced significantly. The difference is that in this case, the electrical field is negative in the upstream of the main channel and positive in the downstream of the main channel, and therefore, the particles will be trapped in the downstream segment of the main channel. We verified this with negatively charged single polystyrene beads of 4 μm in diameter (Bangs Laboratories, Inc, IN). Here we used 4 μm in diameter beads to demonstrate trapping of individual particles. An electrical bias of 5 V was applied to the main channel to induce electroosmotic flow and introduce the particles into the main channel. Then different positive gate voltages (e.g., 20, 30, 40, and 50 V) were applied to the middle reservoir of both side channels.
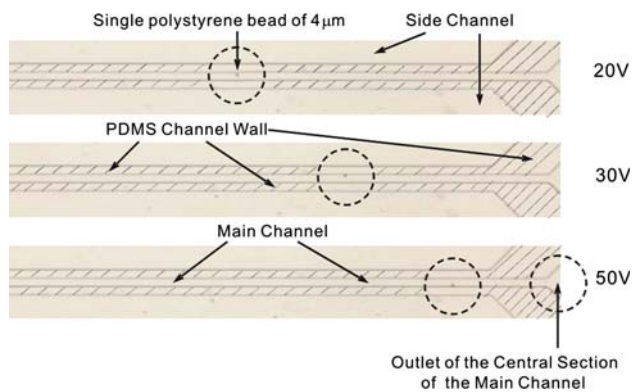
Fig. 10 Images of the microbead trapped using the current leakage from a positive applied voltage applied to the side channel

Fig. 11 Schematic of microfluidic chip for AC pumping with current leakage in the PDMS structure. $L1 = 100$ μm, $L2 = 500$ μm, $d = 15$ μm, and $l = 25$ μm

As expected, we observed that the particles were trapped at different locations in the downstream section of the main channel. Figure 10 shows the images of particle trapping under different applied positive gate voltages.

Compared to other particle manipulation and trapping techniques in the literature, the particle trapping and manipulation technique presented in this paper has advantages including simple design and fabrication without the need of metal electrodes, low-cost, and ease of control by simply adjusting gate voltage. Potential applications of this trapping system include positioning and translocation of single cells. However, the leakage phenomena are not consistent in magnitude and may vary from chip to chip at the present stage, which requires trial and calibration of individual devices before applying them to perform desired functions.

3.4 AC electroosmotic pumping

Based on the previous characterization of electrical current leakage through the PDMS channel walls, in this section, we further show the possibility of generating AC electroosmotic motion by controlling the gate voltage applied at the side channels. This removes the need of patterning electrodes in the microchannels and significantly simplifies the device fabrication. In addition, this provides opportunities of using AC electroosmotic flow to handle molecules that are not compatible with metal electrodes.

Figure 11 shows the schematic of the PDMS microchip to demonstrate AC electroosmotic pumping. Two side channels are separated from the main channel with a 15 μm (d) thick wall and separated from each other with a gap (l) of 25 μm in width. In the experiments, 100 and 1 mM KCl solutions were filled into the side channels and the main channels, respectively. Meanwhile, 500 nm fluorescent micro-particles were added into the main channel to trace the fluid flow. The AC voltage was supplied by a function generator (DS345, Stanford Research Systems, CA). The
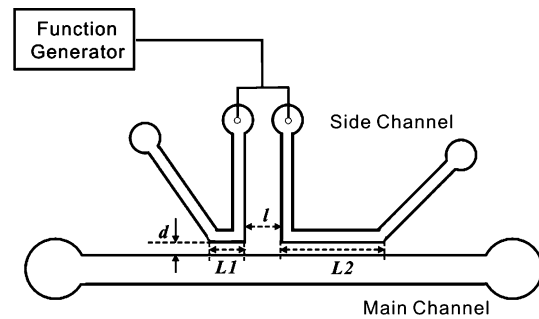
fluorescent image of fluid flow was acquired by an optical microscope.

AC electroosmotic flow has been demonstrated extensively in many recent publications (Green et al. 2000; Gonzalez et al. 2000; Green et al. 2002). Conventionally, to generate a directional net flow using AC electroosmosis, asymmetric microelectrodes must be used (Ajdari 2000; Brown et al. 2000). Equivalently, the asymmetric side channels in Fig. 11 provide such a pair of asymmetric microelectrodes through current leakage.

The model of the AC electroosmotic flow in the microfluidic channel was solved numerically. The potential in the electrolyte satisfies the Laplace's equation

$$\nabla^2 V = 0, \tag{6}$$

with boundary condition outside the EDL on the electrode surface.

$$\sigma \frac{\partial V}{\partial n} = \mathrm{i}\omega C_{\mathrm{EDL}}(V - V_0), \tag{7}$$

where C_{EDL} is the capacitance per unit area of EDL and V_0 is the potential applied to the electrodes. Electric insulation condition $\frac{\partial V}{\partial n} = 0$ is applied to all other boundaries. The real and imaginary parts of the complex potential are then coupled through boundary condition (7) and solved together. Once the Laplace's equation was solved, the mass conservation and Navier–Stokes equation were used to simulate the flow field.

$$\nabla \cdot \vec{u} = 0, \tag{8}$$

$$\rho \vec{u} \cdot \nabla \vec{u} = -\nabla P + \eta \nabla^2 \vec{u}, \tag{9}$$

The Helmholtz–Smoluchowski slip velocity at the electrode surface is used as the boundary condition for the velocity:

$$u = \frac{\varepsilon}{\eta} \Delta V E_x, \tag{10}$$

where ΔV is the difference between the potential across the EDL on the electrodes and E_x is the tangential electric field.
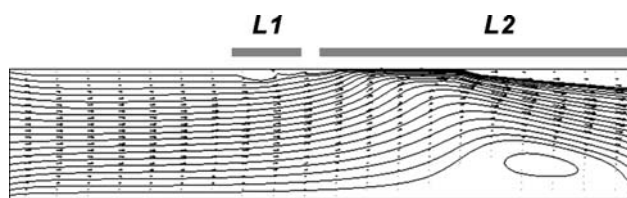
Fig. 12 Modeled results of the flow field in the main channel under the applied AC electrical potential to the asymmetric side channels
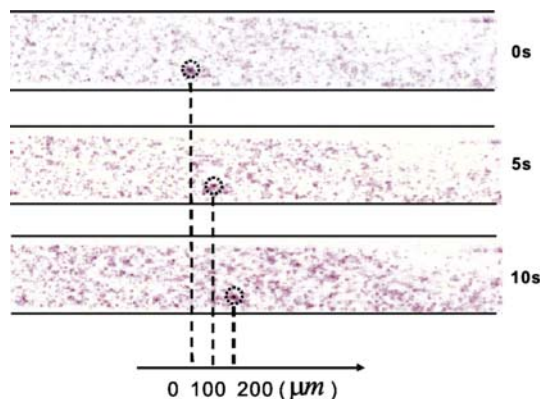

Fig. 13 Fluorescence visualization of the AC pumping experiment. The average speed is estimated to be about 20 μm/s

Figure 12 shows the velocity vectors and streamline from the numerical simulation for the microdevice in Fig. 11. A small vortex is generated in the main channel underneath the narrow side channel on the left and then merges into the bulk flow to the right. This flow pattern qualitatively agrees with those in the literature (Brown et al. 2000). The asymmetric pair electrodes produce a net flow from left to right.

This phenomenon has been experimentally verified with the microfluidic device shown in Fig 11 by observing the flow of the 500 nm fluorescent microparticles suspended in 1 mM KCl solution using an optical microscope. Figure 13 shows three snapshots, taken consecutively every 5 s from a video showing the net motion of fluorescent particles under the AC voltage of ±10 V at 10 kHz applied to the side channels. By highlighting a salient microparticle (circled for illustration in Fig. 13) and tracking its movement, an average flow velocity was estimated to be 20 μm/s by dividing the translocation distance by the corresponding time cost.

4 Conclusions

We have characterized the electrical current leakage through thin PDMS microfluidic channel walls and shown that the leakage current can significantly alter the electric field in the main channel. However, we found that it was difficult to produce significant field-effect control of the zeta potential through tens of microns thick PDMS walls using low gate voltages, different from the published results in the literature. It is demonstrated that utilizing the electrical leakage through the thin PDMS channel walls, we can trap individual particles by balancing the electroosmotic flow and the electrophoretic migration of the particle. In addition, by designing asymmetric side channels, we can generate AC electroosmotic flow inside the main channel.

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