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Alternating-current induced thermal fatigue of gold interconnects with nanometer-scale thickness and width

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With dramatic reduction in sizes of microelectronic devices, the characteristic width and thickness of interconnects in large-scale integrated circuits have reached nanometer scale. Thermal fatigue damage of so small interconnects has attracted more and more attentions. In this work, thermal fatigue of Au interconnects, 35 nm thick and 0.1–5 μm wide, is investigated by applying various alternating current densities to generate cycling temperature and strain in them. A multi-probe measuring system is installed in a scanning electron microscope and a probe-type temperature sensor is for the first time introduced into the system for real-time measuring the temperatures on the pads of the tested interconnects. A one-dimensional heat conduction equation, which uses measured temperatures on the pads as boundary conditions and includes a term of heat dissipation through the interface between the interconnect and the oxidized silicon substrate, is proposed to calculate the time-resolved temperature distribution along the Au interconnects. The measured fatigue lifetimes are presented versus current density and thermal cyclic strain, and the results show that narrower Au lines are more reliable. The failure mechanism of those Au interconnects differs from what is observed in thick interconnects with relatively larger grain size. Topography change caused by localized plasticity on the less-constrained surfaces of the interconnects have not been observed. Instead, grain growing and reorienting due to local temperature varying appear, and grain boundary migration and mergence take place during high temperature fatigue in such thin and narrow interconnects. These results seem to reflect a strain-induced boundary migration mechanism, and the damage morphology also suggests that fatigue of the interconnects with decreased grain size and film thickness is controlled by diffusive mechanisms and interface properties rather than by dislocation glide. Open circuit eventually took place by melting at a region of severely damage cross-sectional area with the grain growing and reorienting. © *2011 American Institute of Physics*. [doi:10.1063/1.3650459]

I. INTRODUCTION

With dramatic reduction in sizes of microelectronic devices, the characteristic width of interconnects in large-scale integrated circuits has reached 32 nm or even below. Such small interconnects will inevitably suffer from thermal fatigue during their manufacture and applications which usually involve extreme conditions such as high temperatures, high current densities, and large thermal strains. The consequent damages caused by electromigration, stress-induced voiding, and thermal fatigue will harm reliability of the interconnects. In the past few decades, there were many researches on the electromigration and stress-induced voiding, typical works such as Refs. 1–5. Although thermal fatigue of interconnects was reported by Philofsky *et al.*[6] in 1971 already, a related experimental research has been hindered by the tiny sizes of the structures. Recently, concerns have been raised about thermal fatigue in much smaller structures, where cyclic thermal strains due to Joule heating can lead to more severe damage of thermal mechanical fatigue in the micro- or nanoscale interconnects with significantly different fatigue behaviors from their bulk counterparts.

Researches on thermal fatigue problems of interconnects have been really developed since the work of Keller *et al.*[7] in 2002. They studied a damage generated by ac currents at 100 Hz in interconnects and mechanical fatigue damage in thin films, finding that the damages by either thermal or mechanical fatigues were similar in nature. In both cases, the damage was caused by surface wrinkles within single grains which grew in amplitude and extent with time. An important progress was made in 2004 by Mönig *et al.* who proposed a new measuring method, four-probe method based on a scanning electron microscope (SEM) stage[8]. They studied thermal-fatigue behaviors of unpassivated Cu lines and pointed out that the fatigue damage was strongly dependent on the film thickness and grain size. Mönig *et al.* also investigated influences of materials[9] and ac frequency[10] on the thermal-fatigue damage of Cu interconnects in 2006 and 2007, respectively. Following Mönig's experimental method, Moreau *et al.*[11] found that the narrower the Cu lines were, the more reliable they were. Meanwhile, they also found that the self-aligned barrier could heighten the lifetime of the Cu lines. More recently, Zhang *et al.*[12] investigated fatigue behavior of Cu interconnects but concluded that the narrower lines had weaker resistance to thermal fatigue. At the same time, Wang *et al.*[13] evaluated thermal-fatigue properties of Au interconnects 50 μm long, 2 μm wide, and 200 nm thick.

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They proposed a simplified one-dimensional heat conduction equation to predict the temperature distribution in the Au interconnect and found that the lifetime of the narrow Au lines still followed the conventional Coffin–Manson relationship if the thermal cyclic strain range was smaller than 0.47%.

There are still some problems unclear, such as how thermal fatigue behavior depends on the electrical current density and the line width, and how the thermal fatigue will behave when the film thickness is further reduced to even the same as the grain size in the lines.

In this paper, a study is carried out on thermal-fatigue behaviors of ultrathin and ultrafine Au interconnects (20 μm long, 0.1–5 μm wide, and 35 nm thick). The thermal fatigue is induced by ac with root mean square (rms) current density from 3.4 to 35.2 MA cm^{-2}. A multi-probe measuring system is developed and employed to perform thermal fatigue tests and a probe-type temperature sensor (probe-T) is introduced to *in situ* measure the temperature of the interconnect pad. A one-dimensional analytical method is proposed to estimate temperature distribution in the Au interconnect. Dependence of the fatigue lifetime on current density and thermal cyclic strain is determined and the different failure mechanism of the Au interconnect from that observed in thick interconnects is analyzed according to the experimental results.

The main reason for us to focus on the behavior of Au nanometer-scale interconnects is to such thin interconnects, the surface oxide layer will seriously affect the mechanical behavior of interconnects when they are exposed to air or heated environment. However, to the Au thin film, it is more difficult to be oxidized in such environments, which provides us an opportunity to investigate the mechanical properties of thin film itself. The other reason is that Au ultrathin films have also extensive applications in microelectronics, laser technology and other function materials. Thermal and mechanical coupling behavior of the Au thin film at nanometer scale is also an important issue.

II. EXPERIMENT DETAIL AND TEMPERATURE FIELD ANALYSIS

Single-level test structures were fabricated by using conventional film deposition and patterning methods. First, a 35 nm thick Au film was deposited onto ⟨100⟩ silicon wafers by electron-beam evaporation. Then, Au interconnect lines with pads at both ends were fabricated by using electron beam lithography. The mean grain size of the Au film was estimated as 32.4 ± 11.9 nm by using linear intercept measurement method,[14] as shown in Fig. 1(b). To determine whether the single-layer grain, a side view SEM morphology image (inclining 85° in imaging) of an interconnect is shown in Fig. 1(c). The SEM image indicates a single layer grain along the interconnect thickness which is about 34.86 nm and very consistent with the deposition thickness. Note, the bright global-like points along the side of the interconnect line are residual gold particles after cooling during the electron beam lithography. The tested lines were 20 μm long, 100 nm to 5 μm wide, and 35 nm thick, each with a pad at either end.

The underlying concept of the method is use of Joule heating controlled by alternating currents to introduce temperature cycles in the interconnects.[7,8] The temperature cycles, in combination with the unavoidable mismatch between thermal expansions, lead to cyclic strains in the interconnect and eventually to its damage.

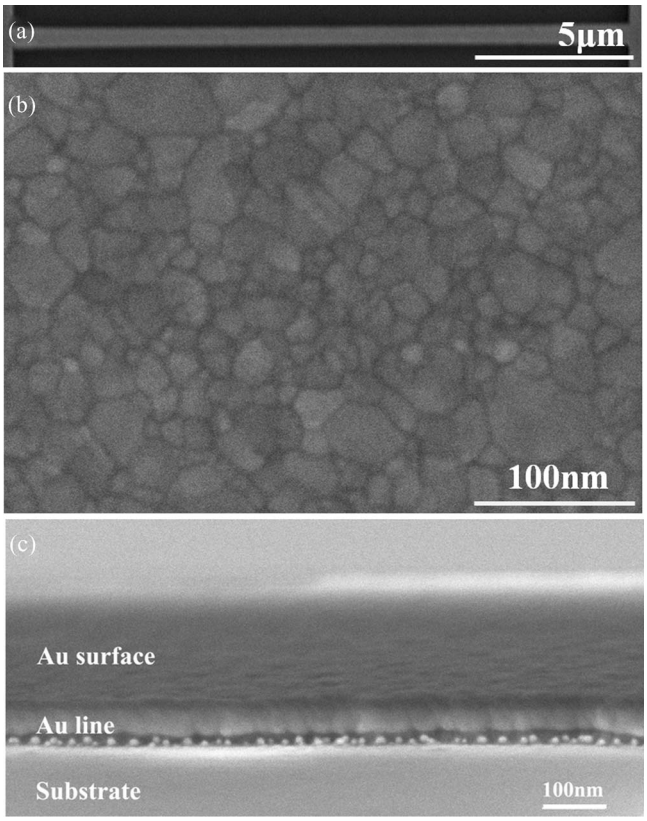

FIG. 1. (a) A tested Au line 35 nm thick and 500 nm wide. (b) Morphologies of its pad surface by SEM imaging. (c) Morphologies of its side face by SEM imaging at a depression angle of 85°.

Thermal fatigue testing of Au interconnects was conducted *in situ* in a SEM (FEI Quata 200F). The wafer containing the interconnects were attached to the sample stage of the SEM. A four-probe unit with Pt needles was controlled by micromanipulators (Kleindiek Nanotechnik) to feed the 100 Hz sinusoidal alternating voltages to the interconnects. The time-resolved voltage $U(t)$ and current $I(t)$ in the test line were identified by a digital oscilloscope (TEK.1002B) and a Source Meter instrument (Keithley 2400), and the resistances of the lines were determined with a time-resolved four-point resistance method. Surface morphologies of the samples during thermal fatigue were monitored by the SEM. In the experiment, the rms density of the applied alternating currents varied from 3.5 to 35.2 MA cm^{-2}, which was expected to generate a temperature cycle with a range of ΔT in the Au interconnects.

Cycling temperature is an important parameter for determining thermal mismatch strains of the interconnects. It is clear that the temperature of the interconnect and its substrate underside would increase owing to the applied alternating current. In the pre-researches, only the substrate temperature has been measured with a thermocouple. In order to get more accurate temperature in the tested lines, a probe-type temperature sensor is introduced into the system to real-time

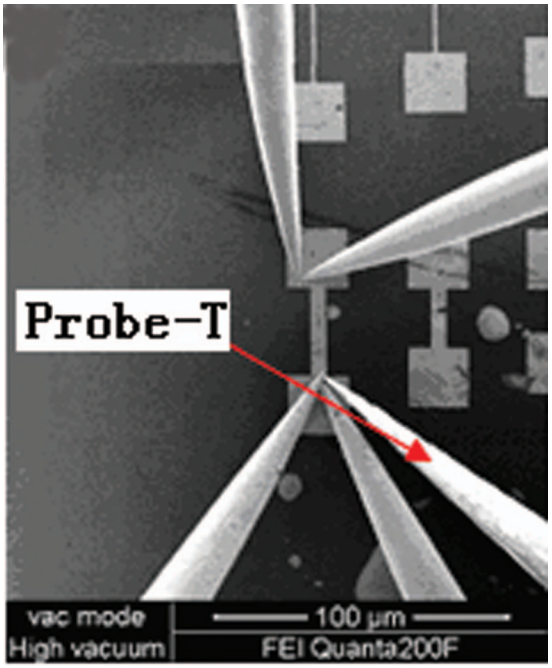

FIG. 2. (Color online) Four-probe and probe-T inside the chamber of a SEM.

measure the temperature on the pad of the tested interconnect at different current densities. The probe-T consists of a thermocouple element and a tungsten tip is controlled by a micromanipulator to accurate position and reliable measurement. Figure 2 shows the multi-probe testing unit. The probe-T was calibrated before the measurements, which is carried out by measuring the same temperature of a heat source with the probe-T and a standard digital thermocouple in a given temperature range. Then the measurement values of the standard thermocouple and the probe-T are compared to complete the calibration. The temperature range in the calibration is from room temperature to 325 °C.

The tested Au interconnects experienced a temperature increase due to Joule heating. Evolution of the temperature in the pad of a 5 μm wide interconnect was measured by probe-T as shown in Fig. 3(a). The temperature increased rapidly at beginning and then gradually stabilized at about 41 °C.

Taking into account the vacuum experimental environment, it is assumed that ac-generated Joule heat in the Au line disperses mainly by heat conduction both towards the pads and the substrate. Therefore, temperature distribution in the interconnect line can be determined accordingly. Applying the first law of thermodynamics:

$$\Delta U = \Delta Q - W, \tag{1}$$

where ΔU is the change in internal energy of the Au line, ΔQ is the heat input to the line, which is equal to the input electric power minus the dispersed heat, and W is the work performed by the line on its surroundings, which is equal to zero in our case. According to Fourier's law, the heat dispersing into the substrate can be calculated as

$$\Delta Q_{ex} = \frac{\lambda_{\mathrm{Si}} \cdot A \cdot \Delta T}{d}, \tag{2}$$

where λ_{Si} is the coefficient of thermal conductivity of the Si substrate (the silicon dioxide layer between the Au line and the Si substrate is neglected for its thickness is much less than that of the silicon substrate), A can be written as $dx \cdot w$ (w is the width of the line, dx is the position change along the line length direction), d is the thickness of the substrate and ΔT is the temperature difference between the Au line and the lower side of the substrate. In Cartesian coordinate system, Eq. (1) can be expressed by

$$\rho c \cdot \frac{\partial T}{\partial t} = \frac{P(t)}{V} + \lambda \frac{\partial^2 T}{\partial x^2} - \frac{\lambda_{\mathrm{Si}} \cdot \Delta T}{d \cdot d_{\mathrm{Au}}}, \tag{3}$$

where ρ is the density, c and λ are specific heat and coefficient of thermal conductivity of the Au line, respectively. The initial and boundary conditions are given as $T(x,0) = f(0)$; $T(0,t) = T(\mathrm{end}, t) = f(t)$, where $f(t)$ is the temperature data of the pad measured by probe-T in the experiments. Substituting testing data $U_{pp} = 1.05$ V, $w = 5$ μm into Eq. (3), the temperature as a function of the position and the time in the line can be solved,

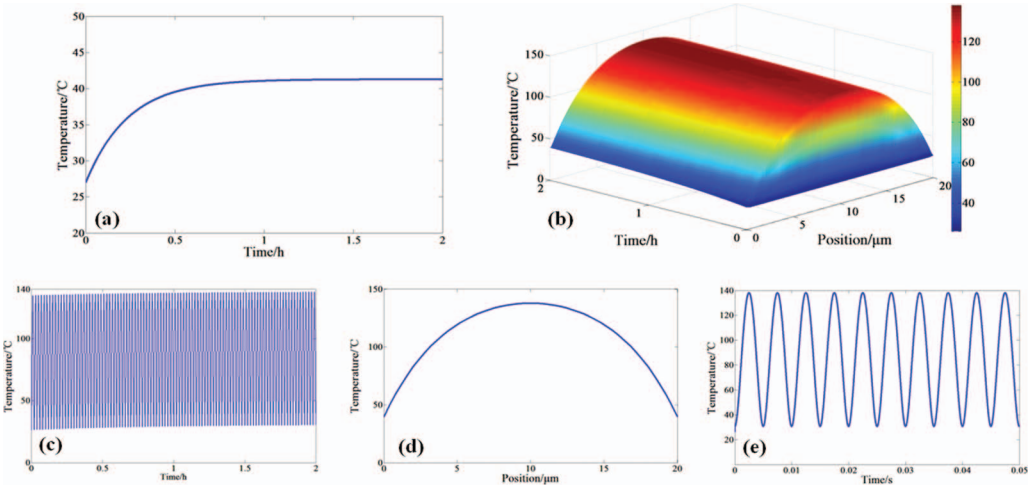

FIG. 3. (Color online) (a) Evolution of the temperature on the pad of the interconnect measured by probe-T. (b) Time-dependent temperature distribution in the interconnect. (c) Temperature evolution at the middle of the interconnect line. (d) Maximum temperature distribution along the line. (e) Temperature evolution at the middle for a very short time period.

and presented in Figs. 3(b)–3(e), where (b) is time-dependent temperature distribution in the interconnect, (c) is the temperature evolution at the middle of the interconnect line, (d) is the maximum temperature distribution along the line, and (e) is the temperature evolution at the middle for a very short time period.

III. RESULTS AND DISCUSSIONS

The Au line suffers from a temperature cycling because of alternating current loading. The temperature at the middle of the line is higher than that at the pads owing to the different heat releases, as shown in Fig. 3(d). Such a temperature distribution is also proved by the experimental fact that almost all of the open circuit failures occur in the middle of the lines. The temperature curve shown in Fig. 3(c) is expanded in Fig. 3(e), where we find that the maximum and minimum temperatures in this line are 138 °C and 30 °C, respectively. Namely, the temperature in the middle of the line changes as a sine wave with an amplitude of 108 °C and a frequency of 200 Hz, which is twice of the ac frequency. The cycling temperature ranges of the tested Au lines with different widths were calculated for varies current densities as shown in Fig. 4. The relationship between the temperature amplitude and current density is fitted to possess a quadratic variation,

$$\Delta T = 0.4268 j^2 + 21.99. \tag{4}$$

On the other side, to the Joule heating mechanism, the temperature range $\Delta T$is proportion to the absorbed energy per volume, i.e.,

$$\Delta T \propto \frac{I^2 R}{V} = \sigma j^2, \tag{5}$$

where σ is the resistivity of the interconnect. Thus, the same relationship between j and $\Delta T$is obtained with Eqs. (4) and (5).

Lifetime of the lines was measured in the experiments at various current densities. Here the failure time is defined as when a line electrically opens. Figure 5(a) shows the dependence of the failure time on current density for different line

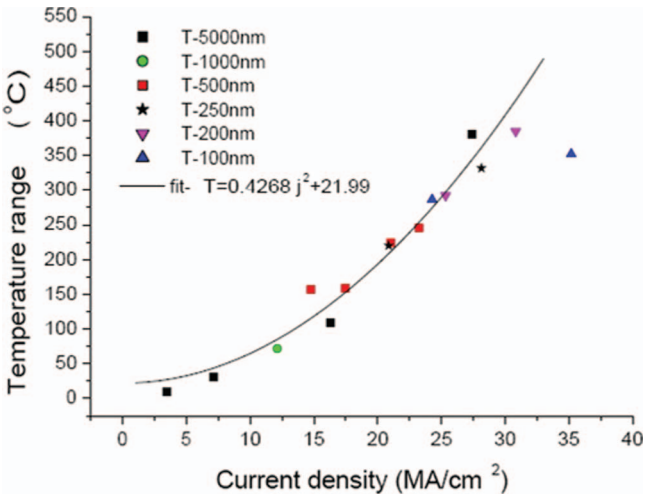

FIG. 4. (Color online) Temperature ranges of the tested lines with different widths at various current densities.

widths. There is only one sample that was used for each point in the curves. Each lifetime of the samples is just the true lifetime at each stress condition. A similar trend is revealed that lifetime is reduced with the current density increasing, and the narrower Au line is more reliable. These results are consistent with the conclusions of Moreau *et al.*[11]

Strain cycles in the line are caused accordingly because of the different thermal expansion coefficients of Au ($\alpha_{Au} = 1.42 \times 10^{-5} K^{-1}$) and SiO_2 ($\alpha_{SiO_2} = 5.7 \times 10^{-7} K^{-1}$). The strain range can be estimated through the temperature range as $\Delta\varepsilon = \Delta T \cdot (\alpha_{Au} - \alpha_{SiO_2})$. The dependence of the cycles' number for failure on the strain range is also presented for the tested lines in Fig. 5(b). All fatigue cycles of the tested lines are over 10^4, which can be called high cycle fatigue.

The surface failure evolution of the Au interconnect lines are observed in SEM images and some typical features are revealed. At first, the failure always occurs in the middle of the interconnects with different widths, and no surface modification, especially wrinkles originating from individual grains as reported in previous works,[12,15] has been observed in the present ultrathin and ultrafine lines which have only a single layer of grains along their thickness. About the open failure occurring in the middle, our analysis has revealed that the temperature level as well as its range at the middle of the line is much higher than that near the pads because heat release is much easier at the ends, where the pads have relatively large areas contacting with the silicon substrate. As to the thermal fatigue damage morphologies shown in Figs. 6 and 7 for 500 nm and 250 nm wide interconnects, where no wrinkles are visible, it can presumably be attributed to the increase in yield stress with decreasing dimensions. Especially, the nanograined film has higher strength and such refined grain size could suppress the dislocation movement and delay damage nucleation.

Figures 6(a) and 6(b) show the 500 nm wide Au line, respectively, in its original state and failed state after 3×10^5 circles ac loading at the strain range $\Delta\varepsilon = 0.33\,\%$. Its surface modifications reveal a new failure mechanism of grain reorientation and non-uniform growth. Views of the square regions marked in Fig. 6(b) are enlarged successively in Figs. 6(c)–6(h) to show more clearly the surface evolution and local thermal fatigue damage morphologies. The morphology near the pad is similar to its original state without growing of the grain sizes (Fig. 6(e)). However, the surface morphologies have been modified seriously in other regions with significant growing of the grains (Fig. 6(f)–6(h)). Obviously, the diverse damage behaviors at the different positions of the Au line are related to the different amplitudes of thermal cyclic temperature or strain. Thermal cycles generated by the ac in the Au cause temperature rising as well as temperature gradient in width and length directions, which in turn lead to the grains growing towards both in width and length directions. Various amplitudes of the temperature in the line lead to different grain scales in different regions. The grain sizes in Figs. 6(f)–6(h) are greater than that in Fig. 6(e) for higher temperature will accelerate diffusion and make the grain growing more easily. Orientated and non-uniform grain growth leads to intergranular microcracks and microvoids, which reduce the strength of the interconnect line to speed up the open-

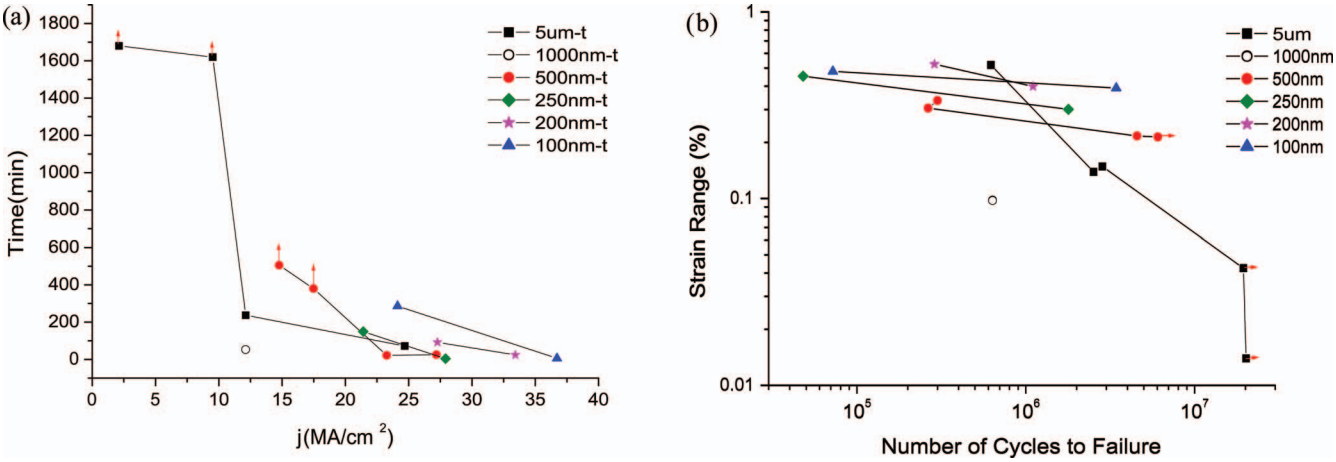

FIG. 5. (Color online) (a) Dependence of the failure time on applied current density for different line widths. (b) Strain range versus the number of cycles to failure. Red arrows indicate that the interconnect lines have not reached failure yet at the end of the experiments.

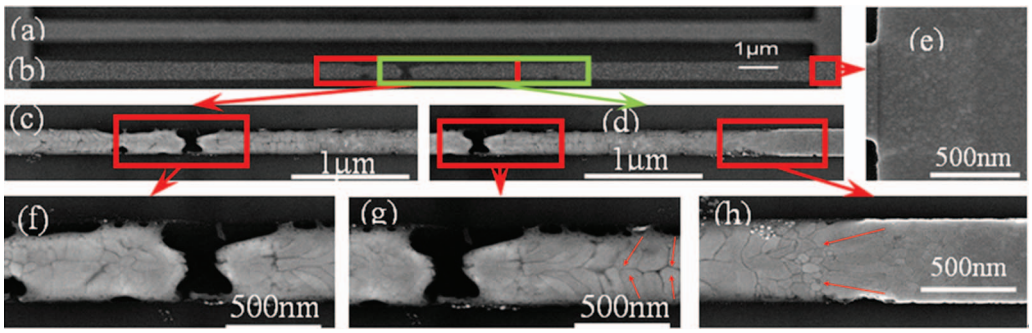

FIG. 6. (Color online) (a) SEM image of 500 nm wide line before loading. (b) The damage image of the same line after ac cycle loading. (c)–(h) Enlarged views of the regions which are marked in (b). Orientated and non-uniform grain growth can be observed clearly with intergranular microcracks and microvoids in the pictures.

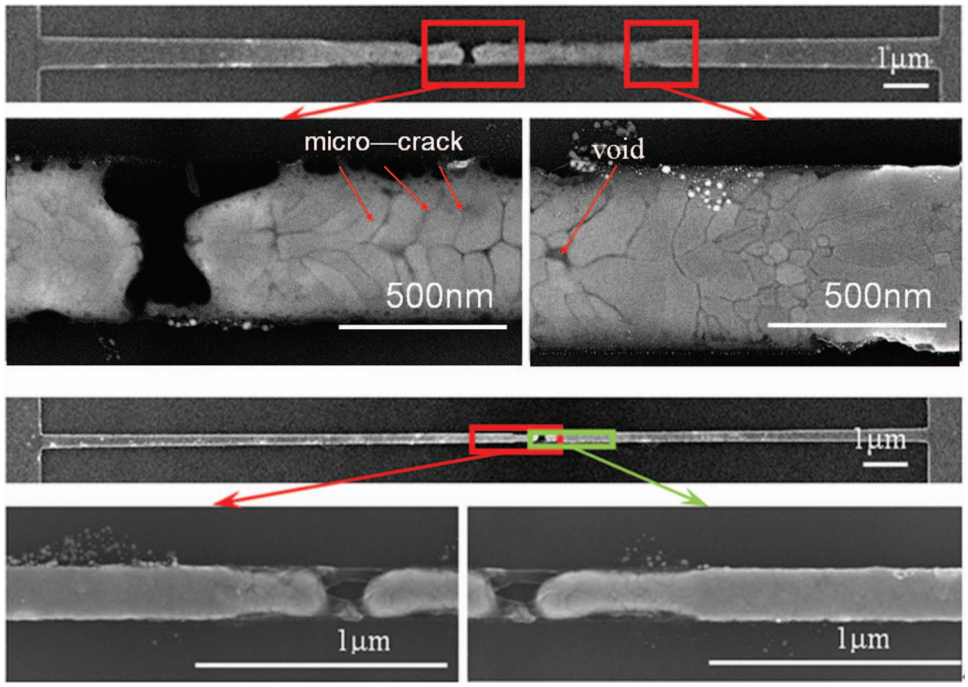

FIG. 7. (Color online) Postmortem SEM pictures of 500 nm (a) and 250 nm (b) wide Au lines. Relative larger grains appear in the wider interconnects.

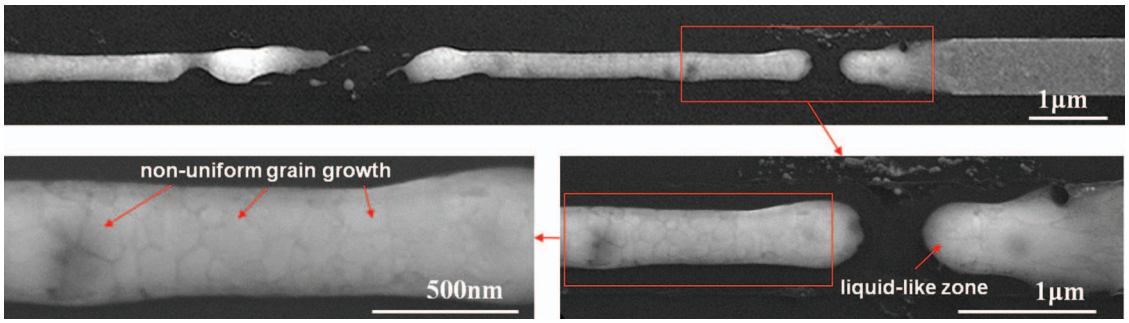

FIG. 8. (Color online) Non-uniform grain growth and grain boundary disappearing to form a liquid-like zone by SEM.

circuit failure. In addition to observing the bamboo-like grains caused by the grain reorientation and non-uniform growth, other types of grains are also observed in our experiments, such as non-uniform grain growth and grain boundary disappearing to form a liquid-like zone (Fig. 8).

According to all these experimental results, the degradation mechanism can be synthesized as follows. With the number of cycles increasing, the Au line exhibits an obvious reduction in resistance to thermal strain mainly due to surface modification, such as grain reorientation and growth, and line section reduction. When a critical number of cycles is reached, electric resistance of the Au line will dramatically increase and lead to a local melting and failure. Concerning effects of the line width, the trend shown in Fig. 5 is that the narrower the Au lines are, the more reliable they are. Presumably, this result can be attributed to the reorientation grain growing with new microcracks and voids produced in relatively larger current density. The wider interconnects do have a larger grain growth (Fig. 7), which may lead to larger defects associated with local non-uniform stress/strain and lower strength of the lines. We may call such a failure mechanism as grain growth degradation for ultrafine films with only a single layer of grains along their thickness.

The surface failure evolution of the Au interconnects in this paper are compared with the works of Mönig *et al.*,[8] Park *et al.*,[9] and Moreau *et al.*[11] for the Cu interconnects. The strong surface roughness with visible extensive grain growth and wrinkles producing in their thick and wide Cu interconnects are not observed in the present ultrathin and ultrafine Au interconnects. Similarities for the fatigue damage aspect can be found with their observations for the narrow and thin Cu lines, such as no wrinkles producing, and the narrower the lines are, the more reliable they are. These effects can be attributed to the increase in yield stress with decreasing dimensions. However, grain reorientation growing and inducing microcracks and voids are not obviously observed in their experiments.

The grain growth based failure mechanism is also somewhat different from the one reported in Ref. 12, where damage propagation was identified as controlled by the extension of damage bands along the width and length of the line with the process prolonged in wider lines. Such damage-propagation-dominated fatigue mechanism should still be responsible for wider lines at a relatively small current density. In the present work, however, relatively larger current densities are chosen so that the experiments can be completed within an acceptable time. Besides, a failure based on dislocation slide fatigue mechanism does also not appear in our experiments, demonstrating the existing conclusion that the thinner metal interconnects will exhibit diffusive fatigue rather than dislocation slide under relatively larger current density.[8]

In addition, the electromigration-induced damage is not considered in the paper. Because the typical characteristics of electromigration[16] which is the transport of material, such as voids, hillocks, and whiskers, are not found in topographical SEM images of the tested lines.

IV. CONCLUSIONS

Fatigue behaviors of Au lines 35 nm thick and 5 μm to 100 nm wide were investigated *in situ* under alternating-current induced cycles inside a SEM chamber. A temperature probe was added to the four-probe scheme for real-time measuring the temperature on the line pad. And the temporal temperature distribution along the Au line was calculated by a one-dimensional heat conduction equation which was combined with the measured temperatures on both ends as boundary conditions and a term of heat dissipation through the interface between the interconnect and the oxidized silicon substrate. The data reported here suggest that under relatively large current densities as used in this work, narrower interconnect lines have stronger resistance to thermal fatigue because reorientated grain growth is more serious in wider lines to weaken their strengths as shown by the postmortem SEM pictures, from which it can be seen that under relatively larger current densities, fatigue damage of the Au lines was dominated by grain growing and ends in melting by excessive Joule heat.

ACKNOWLEDGMENTS

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